

**REMARKS**

Claims 1-24 are pending. Claims 5 and 14-17 have been withdrawn from further consideration as being directed to a non-elected invention. Claims 6-13 and 18-20 have been allowed.

Claims 1, 2 and 21-23 were rejected under 35 USC §103(a) as being unpatentable over Edmond et al. in view of Nakamura et al.; and claims 4 and 24 were rejected under 35 USC §103(a) as being unpatentable over Edmond et al, Nakamura et al. and further in view of Powell et al. Favorable reconsideration of these rejections is earnestly solicited.

The Examiner acknowledges that Edmond et al. fails to disclose the claimed carrier concentration, and applies Nakamura et al. for allegedly rendering the claimed carrier concentration obvious. The Examiner does not comment on the limitations added to claims 1 and 21 in the Preliminary Amendment filed on April 30, 2002. That is, the Examiner does not comment on the limitations of “so as to reduce an interface resistance between said substrate and said buffer layer” in claim 1 and “so as to reduce an interface resistance between said SiC substrate and said AlGaN layer.”

The portion of Nakamura et al. highlighted by the Examiner at column 14, line 3 relates to a carrier concentration of the first clad layer 16 (not the buffer layer) which does not make a direct contact with the substrate 12. Even if one of ordinary skill in the art would have substituted a substrate of SiC based on Nakamura et al.’s description at column 6, line 2, there

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would be no interface between such a SiC substrate 12 and the first clad layer 16 of Nakamura et al. as required by claims 1 and 21. Thus, since the carrier concentration described by Nakamura et al. does not relate to lowering of the interface resistance between the AlGaIn buffer layer and the SiC substrate acting as a current path, the combination of the teachings of Edmond et al. and Nakamura et al. would not have rendered the claimed invention obvious which requires reducing an interface resistance.

Furthermore, there is no current path at the interface between the substrate and the buffer layer of Nakamura et al. As such, it would not be possible to combine the teachings of Nakamura et al. with Edmond et al. in a manner such that the injected current is caused to flow from the substrate 21 or 41 to the buffer layer 22 or 42 across the substrate/buffer layer interface. One of ordinary in the art would not have been motivated to make the modifications urged by the Examiner.

For at least the foregoing reasons, the claimed invention distinguishes over the cited art and defines patentable subject matter. Favorable reconsideration is earnestly solicited.

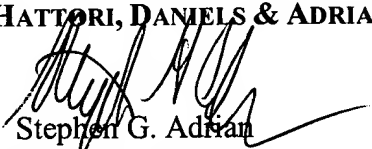
Should the Examiner deem that any further action by applicants would be desirable to place the application in condition for allowance, the Examiner is encouraged to telephone applicants' undersigned attorney.

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If this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. The fees for such an extension or any other fees that may be due with respect to this paper may be charged to Deposit Account No. 50-2866.

Respectfully submitted,

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